



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

10/667,615

09/22/2003

Theodore W. Houston

TI 35657

1175

23494 7590 10/09/2007
TEXAS INSTRUMENTS INCORPORATED
P O BOX 655474, M/S 3999
DALLAS, TX 75265

EXAMINER

ARENA, ANDREW OWENS

ART UNIT

PAPER NUMBER

2811

NOTIFICATION DATE

DELIVERY MODE

10/09/2007

ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

uspto@ti.com
uspto@dlemail.itg.ti.com

Office Action Summary	Application No.	Applicant(s)	
	10/667,615	HOUSTON, THEODORE W.	
	Examiner	Art Unit	
	Andrew O. Arena	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 12 July 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1, 3, 5-7, 9-14, 17 and 19-26 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1, 3, 5-7, 9-14, 17 and 19-26 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

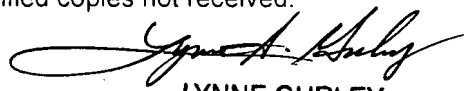
Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.


LYNNE GURLEY
SUPERVISORY PATENT EXAMINER
AU 2811, TC 2800

Attachment(s)

- | | |
|--|---|
| <p>1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)</p> <p>2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)</p> <p>3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
 Paper No(s)/Mail Date _____</p> | <p>4) <input type="checkbox"/> Interview Summary (PTO-413)
 Paper No(s)/Mail Date. _____</p> <p>5) <input type="checkbox"/> Notice of Informal Patent Application</p> <p>6) <input type="checkbox"/> Other: _____</p> |
|--|---|

DETAILED ACTION

The indicated allowability of claims 9&12 and of claims 17-19 is withdrawn in view of the newly discovered references to Chau (US 2004/0036126) and Fazan (US 2005/0017240), respectively. New rejections not necessitated by amendment are presented below; accordingly this action is non-final.

Claim Objections

Claims 21 & 22 are objected to; the recitation "gate structure is a fin-fet" is impossible, thus indefinite. A gate cannot be a transistor, only a component thereof. An appropriate recitation is: "gate structure is a tri-gate". Appropriate correction is required.

Claims 17, 19, 21, 23, 25, and 26 are objected to under 37 CFR § 1.75 (i) because each element or step should be separated by a line indentation (length/ratio limitations are separate, further limits to preceding recitations). See corrections herein.

Claim 19 is objected to; it recites "said logic transistor further comprises a logic body region", already recited in parent claim 17. Said recitation should be cancelled.

Claim Rejections - 35 USC § 102

Claims 1, 3, 5, 6, 7, 10, 13, 14, and 21-26 are rejected under 35 U.S.C. 102(e) as being anticipated by Chen (US 6,720,619).

Re claim 1, Chen discloses a memory device, comprising (e.g., Figs 1c & 2):

a body region (body & fin 204; col 4 ln 40) insulated from a substrate;

an insulating layer (110 & 202; col 4 ln 48) on a surface of said body region; and

a gate structure on said insulating layer and conformally surrounding a portion of said body region (col 4 ln 48-50), wherein a width of said body region is sufficient to provide a not fully depleted region (Fig 1c, "partially depleted"; Fig 4, "PD-SOI");

wherein said width of said body region is greater than a length of said gate structure (Fig 1c; shaded "PD-SOI" region in Fig 4).

It seems the body of the claim fully sets forth the claimed invention and the preamble "memory" is not necessary to give the claim meaning, only reciting intended use of a structure otherwise disclosed by the prior art. See MPEP § 2111.02 & 2114.

Re claim 3, Chen discloses said gate structure is a tri-gate (contacts three sides of body region) and a ratio of said width of said body region to said gate length is at least about 1.5:1 (encompassed by Fig 4).

Re claim 5, Chen discloses said body region is insulated from said substrate by an oxide layer (Buried Oxide in Fig 1C).

Re claim 6, Chen discloses said body region is insulated from the substrate by a buried layer of a silicon-on-insulator (SOI) substrate (col 1 ln 8-11; col 3 ln 1).

Re claim 7, Chen discloses a method of manufacturing a memory device (Chen inherently formed the components of the device), comprising (e.g., Figs 1c & 2):

forming a body region (body & fin 204; col 4 ln 40) insulated from a substrate;
depositing an insulating layer (110 & 202; col 4 ln 48) on a surface of said body region; and

forming a gate structure on said insulating layer and conformally surrounding a portion of said body region (col 4 ln 48-50), wherein a width of said body region is sufficient to provide a not fully depleted region ("partially depleted"; Fig 4, "PD-SOI"); wherein said width of said body region is greater than a length of said gate structure (Fig 1c; shaded "PD-SOI" region in Fig 4).

It seems the body of the claim fully sets forth the claimed invention and the preamble "memory" is not necessary to give the claim meaning, only reciting intended use of a structure otherwise disclosed by the prior art. See MPEP § 2111.02 & 2114.

Re claim 10, Chen discloses said body region is formed from a silicon layer of a silicon-on-insulator (SOI) substrate.

Re claim 13, Chen discloses said gate structure is a tri-gate (contacts three sides of body region).

Re claim 14, Chen discloses a ratio of said width of said body region to said gate length is at least about 1.5:1 (encompassed by Fig 4).

Re claim 21, Chen discloses a memory device, comprising (e.g., Figs 1c & 2):
a body region (body & fin 204; col 4 ln 40) insulated from a substrate;
an insulating layer (110 & 202; col 4 ln 48) on a surface of said body region; and
a gate structure on said insulating layer and conformally surrounding a portion of said body region (col 4 ln 48-50), wherein a width of said body region is sufficient to provide a not fully depleted region (Fig 1c, "partially depleted"; Fig 4, "PD-SOI");
wherein said gate structure is a fin-fet (interpreted as a tri-gate, contacting three sides of the channel body), and

wherein a ratio of said width of said body region to a gate length is at least about 1:1 (Fig 1C; encompassed by Fig 4).

It seems the body of the claim fully sets forth the claimed invention and the preamble "memory" is not necessary to give the claim meaning, only reciting intended use of a structure otherwise disclosed by the prior art. See MPEP § 2111.02 & 2114.

Re claim 22, Chen discloses a ratio of said width of said body region to a gate length is at least about 1:1 (Fig 1C; Fig 4). Note; already in claim 22 via claim 21.

Re claim 23, Chen discloses a method of manufacturing a memory device (Chen inherently formed the components of the device), comprising (e.g., Figs 1c & 2):

forming a body region (body & fin 204; col 4 ln 40) insulated from a substrate;
depositing an insulating layer (110 & 202; col 4 ln 48) on a surface of said body region; and

forming a gate structure on said insulating layer and conformally surrounding a portion of said body region (col 4 ln 48-50), wherein a width of said body region is sufficient to provide a not fully depleted region ("partially depleted"; Fig 4, "PD-SOI");

wherein said gate structure is a fin-fet (interpreted i as a tri-gate, contacting three sides of the channel body), and

wherein a ratio of said width of said body region to a gate length is at least about 1:1 (Fig 1C; encompassed by Fig 4).

It seems the body of the claim fully sets forth the claimed invention and the preamble "memory" is not necessary to give the claim meaning, only reciting intended use of a structure otherwise disclosed by the prior art. See MPEP § 2111.02 & 2114.

Art Unit: 2811

Re claim 24, Chen discloses a ratio of said width of said body region to a gate length is at least about 1:1 (Fig 1C; Fig 4). Note; already in claim 24 via claim 23.

Re claim 25, Chen discloses a memory device, comprising (e.g., Figs 1c & 2):
a body region (body & fin 204; col 4 ln 40) insulated from a substrate;
an insulating layer (110 & 202; col 4 ln 48) on a surface of said body region; and
a gate structure on said insulating layer and conformally surrounding a portion of said body region (col 4 ln 48-50), wherein a width of said body region is sufficient to provide a not fully depleted region (Fig 1c, "partially depleted"; Fig 4, "PD-SOI");

wherein said gate structure is a tri-gate structure (contacting three sides of the channel body), and

wherein a ratio of said width of said body region to a gate length is at least about 1.5:1 (Fig 1C; encompassed by Fig 4).

It seems the body of the claim fully sets forth the claimed invention and the preamble "memory" is not necessary to give the claim meaning, only reciting intended use of a structure otherwise disclosed by the prior art. See MPEP § 2111.02 & 2114.

Re claim 26, Chen discloses a method of manufacturing a memory device (Chen inherently formed the components of the device), comprising (e.g., Figs 1c & 2):

forming a body region (body & fin 204; col 4 ln 40) insulated from a substrate;
depositing an insulating layer (110 & 202; col 4 ln 48) on a surface of said body region; and

forming a gate structure on said insulating layer and conformally surrounding a portion of said body region (col 4 ln 48-50), wherein a width of said body region is sufficient to provide a not fully depleted region ("partially depleted"; Fig 4, "PD-SOI");

wherein said gate structure is a tri-gate structure (contacting three sides of the channel body), and

wherein a ratio of said width of said body region to a gate length is at least about 1.5:1 (Fig 1C; encompassed by Fig 4).

It seems the body of the claim fully sets forth the claimed invention and the preamble "memory" is not necessary to give the claim meaning, only reciting intended use of a structure otherwise disclosed by the prior art. See MPEP § 2111.02 & 2114.

Claims 1, 3, 5-7, 9-14, and 21-26 are rejected under 35 U.S.C. 102(e) as being anticipated by Chau (US 2004/0036126).

Re claim 1, Chau discloses a memory device, comprising (e.g., Fig 3 & 5):
a body region (¶37 ln 5-6) insulated from a substrate (¶32 ln 11-12);
an insulating layer on a surface of said body region (¶41 ln 1-6); and
a gate structure on said insulating layer and conformally surrounding a portion of said body region (¶42 ln 1-7 & 12-14), wherein a width of said body region is sufficient to provide a not fully depleted region (Fig 6; ¶27 ln 8-10);
wherein said width of said body region is greater than a length of said gate structure (encompassed by Fig 6).

It seems the body of the claim fully sets forth the claimed invention and the preamble "memory" is not necessary to give the claim meaning, only reciting intended use of a structure otherwise disclosed by the prior art. See MPEP § 2111.02 & 2114.

Re claim 3, Chau discloses said gate structure is a tri-gate (contacts three sides of body region) and a ratio of said width of said body region to said gate length is at least about 1.5:1 (encompassed by Fig 6).

Re claim 5, Chau discloses (Fig 3) said body region is insulated from said substrate by an oxide layer (306; ¶18 ln 7).

Re claim 6, Chau discloses (Fig 3) said body region is insulated from the substrate by a buried layer of a silicon-on-insulator (SOI) substrate (302; ¶16 ln 4).

Re claim 7, Chau discloses a method of manufacturing a memory device, comprising (e.g., Fig 5A-5J; ¶32 ln 1-3):

forming a body region (¶37 ln 5-6) insulated from a substrate (¶32 ln 11-12);

depositing an insulating layer on a surface of said body region (¶41 ln 1-6); and

forming a gate structure on said insulating layer and conformally surrounding a portion of said body region (¶42 ln 1-7 & 12-14), wherein a width of said body region is sufficient to provide a not fully depleted region (Fig 6; ¶27 ln 8-10);

wherein said width of said body region is greater than a length of said gate structure (encompassed by Fig 6).

It seems the body of the claim fully sets forth the claimed invention and the preamble "memory" is not necessary to give the claim meaning, only reciting intended use of a structure otherwise disclosed by the prior art. See MPEP § 2111.02 & 2114.

Re claim 9, Chau discloses said gate length is less than about 35 nanometers (Fig 6; ¶27 ln 4-5).

Re claim 10, Chau discloses said body region is formed from a silicon layer of a silicon-on-insulator (SOI) substrate (¶32 ln 4-17, ¶37 ln 5-6).

Re claim 11, Chau discloses forming said body region includes forming a mask (510) by depositing and patterning a resist over said silicon layer (¶37 ln 1-6) and performing an anisotropic etch to remove portions of said silicon layer not protected by said mask (¶39 ln 6-9).

Re claim 12, Chau discloses said mask is a sidewall structure (must be broadly interpreted, in light of specification, without importing limitations therefrom and therefore reads on Fig 5B as per MPEP § 2111. A "sidewall structure" must be interpreted as spaced apart patterns such as in Chau Fig 5B and applicant's Fig 2E; it would be improper to import any further limitations not recited in the claim, such as applicant's Fig 2D and the several non-recited method steps which connect Figs 2D-2E).

Re claim 13, Chau discloses said gate is a tri-gate (¶32 ln 1).

Re claim 14, Chau discloses a ratio of said width of said body region to said gate length is at least about 1.5:1 (encompassed by Fig 6).

Re claim 21, Chau discloses a memory device, comprising (e.g., Fig 3 & 5):

a body region (¶37 ln 5-6) insulated from a substrate (¶32 ln 11-12);

an insulating layer on a surface of said body region (¶41 ln 1-6); and

a gate structure on said insulating layer and conformally surrounding a portion of said body region (¶42 In 1-7 & 12-14), wherein a width of said body region is sufficient to provide a not fully depleted region (Fig 6; ¶27 In 8-10);

wherein said gate structure is a fin-fet (interpreted as a tri-gate, contacting three sides of the channel body), and

wherein a ratio of said width of said body region to a gate length is at least about 1:1 (encompassed by Fig 6).

It seems the body of the claim fully sets forth the claimed invention and the preamble "memory" is not necessary to give the claim meaning, only reciting intended use of a structure otherwise disclosed by the prior art. See MPEP § 2111.02 & 2114.

Re claim 22, Chau discloses a ratio of said width of said body region to a gate length is at least about 1:1 (encompassed by Fig 6).

Re claim 23, Chau discloses a method of manufacturing a memory device, comprising (e.g., Figs 3 or 5A-5J; ¶32 In 1-3):

forming a body region (¶37 In 5-6) insulated from a substrate (¶32 In 11-12);

depositing an insulating layer on a surface of said body region (¶41 In 1-6); and

forming a gate structure on said insulating layer and conformally surrounding a portion of said body region (¶42 In 1-7 & 12-14), wherein a width of said body region is sufficient to provide a not fully depleted region (Fig 6; ¶27 In 8-10);

wherein said gate structure is a fin-fet (interpreted as a tri-gate, contacting three sides of the channel body), and

wherein a ratio of said width of said body region to a gate length is at least about 1:1 (encompassed by Fig 6).

It seems the body of the claim fully sets forth the claimed invention and the preamble "memory" is not necessary to give the claim meaning, only reciting intended use of a structure otherwise disclosed by the prior art. See MPEP § 2111.02 & 2114.

Re claim 24, Chau discloses a ratio of said width of said body region to a gate length is at least about 1:1 (encompassed by Fig 6).

Re claim 25, Chau discloses a memory device, comprising (e.g., Fig 3 & 5):
a body region (¶37 ln 5-6) insulated from a substrate (¶32 ln 11-12);
an insulating layer on a surface of said body region (¶41 ln 1-6); and
a gate structure on said insulating layer and conformally surrounding a portion of said body region (¶42 ln 1-7 & 12-14), wherein a width of said body region is sufficient to provide a not fully depleted region (Fig 6; ¶27 ln 8-10);

wherein said gate structure is a fin-fet (interpreted as a tri-gate, contacting three sides of the channel body), and

wherein a ratio of said width of said body region to a gate length is at least about 1.5:1 (encompassed by Fig 6).

It seems the body of the claim fully sets forth the claimed invention and the preamble "memory" is not necessary to give the claim meaning, only reciting intended use of a structure otherwise disclosed by the prior art. See MPEP § 2111.02 & 2114.

Re claim 26, Chau discloses a method of manufacturing a memory device, comprising (e.g., Figs 3 or 5A-5J; ¶32 ln 1-3):

forming a body region (¶37 ln 5-6) insulated from a substrate (¶32 ln 11-12);
depositing an insulating layer on a surface of said body region (¶41 ln 1-6); and
forming a gate structure on said insulating layer and conformally surrounding a
portion of said body region (¶42 ln 1-7 & 12-14), wherein a width of said body region is
sufficient to provide a not fully depleted region (Fig 6; ¶27 ln 8-10);

wherein said gate structure is a fin-fet (interpreted as a tri-gate, contacting three
sides of the channel body), and

wherein a ratio of said width of said body region to a gate length is at least about
1.5:1 (encompassed by Fig 6).

It seems the body of the claim fully sets forth the claimed invention and the
preamble "memory" is not necessary to give the claim meaning, only reciting intended
use of a structure otherwise disclosed by the prior art. See MPEP § 2111.02 & 2114.

Claims 17, 19 and 20 are rejected under 35 U.S.C. 102(e) as being anticipated
by Fazan (US 2005/0017240).

Re claim 17, Fazan discloses an integrated circuit, comprising (Fig 17A; ¶41):
a one-transistor dynamic random access memory (1T DRAM) device, including:
a body region (118b; ¶44 ln 6) insulated (114) from a substrate (112, ¶43 ln 1-9);
an insulating layer (120) on a surface of said body region (¶44 ln 10-14); and
a gate structure (124; ¶46 ln 6) on said insulating layer and conformally
surrounding portions of said body region wherein a width of said body region is
sufficient to provide a not fully depleted region ("PD" in ¶54, also ¶¶ 12, 13, 51);

a logic transistor (108x; ¶42 In 9-11) located on said substrate;
wherein said logic transistor is a multigate transistor (¶42 In 9-11) having a logic body region (118a; ¶44 In 6-8),
a width of said logic body region being less than said body width of said 1T DRAM device (¶26; ¶55 In 10-12; just look at Fig 17A); and
interconnects to interconnect said 1T DRAM and said logic transistor to form an operative integrated circuit (¶59).

Re claim 19, Fazan discloses said logic transistor further comprises:
an insulating layer (120) on said surface of said logic body region,
wherein said gate structure (124; ¶46 In 6) is on said insulating layer and said gate structure conformally surrounds portions of said logic body region, and
said gate length is substantially equal to a height and to a width of said logic body region (¶26, ¶54 In 1-3, ¶55 In 10-12; just see Fig 17A).

Re claim 20, Fazan discloses wherein a logic body region of said logic transistor is fully depleted (one of ordinary skill understands this in ¶51 In 5-9; MPEP § 2141.03).
Furthermore, this is intended use of an anticipated structure. See MPEP § 2114.

Response to Arguments

Applicant's arguments filed 07/12/2007 have been fully considered but they are not persuasive.

The arguments that: Chen does not teach the body width to gate length relationship (pg 9 ¶3 In 1-4); that "Fig 4 shows...not the [body width]" (pg 9 last line);

Art Unit: 2811

and that Chen does not disclose the ratio (e.g., pg 11 – pg 12) are not persuasive. The arguments are predicated on the assertion that “Length Lg” and “Width W” of Chen Fig 4 would not necessarily be understood to be the claimed gate length and body width.

A disclosure is directed to one of ordinary skill in the art; Chen is relevant not only for the explicit statements contained therein, but also for anything those statements would have reasonably suggested. MPEP § 2123(I) and § 2164.01 citing to Buchner.

A person having ordinary skill in the art of field effect transistors, of necessity, understands: 1) the relationship between depletion and the gate-channel overlap; and 2) that gate length is measured in the source-to drain direction. See MPEP § 2141.03 citing to Hiyamizu. The fundamental principle of this art is that an inversion region allows current to flow from source to drain through the channel, said region caused a gate overlapping and applying a voltage to said region. See for example Pierret (“Semiconductor Device Fundamentals”) and also Ng, both attached.

Turning now to Chen, as understood in the art, a FinFET has a source at one end of the fin and a drain at the other (e.g., col 4 ln 64-65). Gate length is precisely defined and known to be measured along the fin, and body width is precisely defined and known to be parallel to the substrate surface and perpendicular to the gate length (e.g., Fig 1C compared to Fig 1D, both labeling the width W in this direction).

Chen would be understood to encompass the claimed lengths, widths, and ratios; e.g., Fig 1C with Fig 4. As an explicit example, in Fig 4, following the $L_g=0.6$ data set horizontally, most body widths W are greater than 0.9, and therefore most disclosed ratios are $W:L_g \geq 1.5:1$, all cause partial depletion (“PD-SOI”).

Further evidence of the meaning of gate length and body width can be found in Chau; background (Fig 1; ¶5 ln 3-6) and disclosure (Fig 2, Fig 3; ¶7 ln 6-8, ¶17 ln 4-8).

The arguments that Chen does not teach a tri-gate (e.g., pg 10 ¶2, pg 11 ¶ 3) are not persuasive. It is the structure that is most important in determining patentability, word interpretation is not fixed. Applicant's device (e.g., Figs 1, 2G, 3) and Chen's device (e.g, Figs 1C, 2) depict the same gate structure. The claim language "tri-gate" encompasses Chen because his gate contacts (1) one side, (2) one top, and (3) another side, of the body; regardless of the language chosen by Chen.

A dual-gate is understood to require a spacer on top of the channel fin so that the gate electrode exerts negligible influence thereupon. Chau is but one explicit example of this convention in this art (209 in Fig 2B; ¶6). Therefore, although Chen is free to be his own lexicographer, Chen actually discloses a tri-gate as understood in the art.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Both Yoshida and Houston teach fully-depleted logic integrated with partially-depleted memory on a single IC.

Pierret and Ng are evidence of the level of ordinary skill in the art, and in this case, particularly demonstrate what gate length and body width mean.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew O. Arena whose telephone number is 571-272-5976. The examiner can normally be reached on M-F 8:30-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne A. Gurley can be reached on 571- 272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Andrew O. Arena
26 September 2007



LYNNE GURLEY
SUPERVISORY PATENT EXAMINER
AU 2811, TC 2800